REMARKS

The Examiner is thanked for his Office Action.

The claims presently outstanding are Claims 1-2. New Claims 3-6 (closely based on the summary section of the application as filed) are sought to be added. These changes are believed not to introduce new matter, and their entry is respectfully requested.

Peddada et al.

Peddada et al. suggests texture caching, but does not appear to provide any suggestion of letting the graphics accelerator itself access main memory directly. To the contrary, Peddada et al. appears to center on graphics drivers (i.e. low-level system-side software), rather than processes running on the graphics accelerator itself:

Col.3 *ll.*61ff: (Summary of the Invention): "A graphics driver for an ... AGP personal computer has a set-render process that is called by a high-level application when a texture is ready for rendering.... A handle-texture process is called... before the 3D graphics engine is enabled to render the texture."

Also note that Peddada et al. mentions the "AGP Execute" model, but expressly teaches AWAY from it:

> **Unfortunately, 3D graphics accelerator 20 must have additional hardware to directly access textures from AGP memory 14. This extra hardware adds to the expense and complexity of 3D graphics accelerator 20 AND IS THUS UNDESIRABLE.**
>
> Col.1 *ll.*58-62 (emphasis added)

Porterfield

Porterfield does teach virtual memory operations (within the GART space), but does not suggest that these operations are managed by the graphics accelerator. Indeed it appears that Porterfield only contemplates virtual memory management on the host side, NOT by the graphics accelerator; this appears clearly from many statements in Porterfield, e.g.

Col.7 *ll.*21ff: "In one embodiment, the system logic 154 performs the address remapping...."

Col.8 *ll.*42ff: "In one embodiment, an initialization BIOS implements the GART table... by loading configuration registers in the system logic... during system boot up. In another embodiment, the operating system implements the GART table...."

Col.16 *ll.*62ff: "Referring now to FIG. 11, a flowchart illustrates one embodiment of a process for fetching a GART PTE.... At state 360, the system logic ... obtains the virtual page number ... from the virtual address...."

Analysis of Art Rejections

The art rejections are all respectfully traversed.

Note Claim 1's recitation of "either downloading said textures..., or selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said main memory without downloading them into said graphics memory." As discussed above, NONE of the references of record meet this limitation. Both Peddada and Porterfield use host-side management for accesses to main memory, so that neither meets this limitation.

Also note Claim 2's recitation of "software, integrated on said chip, which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory." Again, the references of record do not appear to show any such function on the graphics chip. Without any such teaching in ANY reference it is hard

to see how the combined references could lead to such a teaching.

Applicant respectfully disputes the Examiner's suggested motive to combine two AGP modes. While the two modes may be separately known, there is NO teaching in the art of record which suggests combining them at all, much less in a way which would meet the claim limitations. The Examiner has not shown any reason why the asserted combination would meet the limitations of Claim 1, nor those of Claim 2.

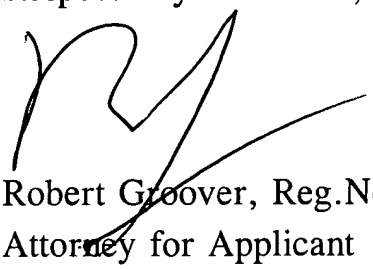
The Examiner's suggestion that it would have been obvious to combine... "in order to use both AGP models" is not supported by any teaching in the art of record: what reference suggests that using both AGP models would be possible, or desirable? Thus Applicant respectfully suggests that the Examiner's assertion is improper hindsight reconstruction, and is not supported by the content of the art.

If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out very specifically where such teaching may be found.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney for an interview to resolve any remaining issues.

Respectfully submitted,



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